Hall Ticket Number:

Code No. : 13606 O3

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (IT) II Year I-Semester Old Examinations, May/June-2018

Digital Electronics and Logic Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Implement the Boolean function F=A(CD+B)+BC' using NAND gates.
2. Write VHDL Program for implementing XOR operation.
3. Give any two differences between PLAs and PALs.
4. Implement an Half adder circuit.
5. Convert D flip-flop to T flip-flop using excitation tables.
6. Give the truth tables and excitation tables of SR and JK flip flops.
7. Differentiate between Mealy and Moore state models.
8. List two differences between synchronous sequential circuits and asynchronous sequential circuits.
9. Differentiate between static and dynamic hazards.
10. Define set up and hold time of a flip-flop.

Part-B (5 × 10 = 50 Marks)

11. a) Minimize and implement $f(x_1, x_2, x_3) = \sum m(1,3,4,7)$ using only NOR gates. [8]
    b) Write short notes on TTL 74 series gates. [2]

12. a) Design a 4 input priority encoder. [5]
    b) Explain Arithmetic comparison circuits. [5]

13. a) Design a 3 bit binary counter using T Flip flop. [5]
    b) Explain JK flip-flop with neat circuit diagram and timing diagram. [5]

14. a) Design a sequential circuit with two D flip flops A and B and one input x. When x = 0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 and back to 00 and repeats. [8]
    b) Write short notes on CAD tools. [2]

15. a) Explain digital hardware design flow. [5]
    b) Explain the different types of hazards in combinational circuits. [5]

16. a) Implement $f(x_1, x_2, x_3) = \sum m(1, 2, 4, 7)$ (i) using 2:1 multiplexers only and (ii) using 4:1 multiplexers only. [7]
    b) Explain the significance of number system. [3]

17. Answer any ***two*** of the following:
    a) Master-slave edge triggered flip-flops. [5]
    b) FSM as an arbiter circuit. [5]
    c) ASM charts. [5]